UC864 Digital Voice Interface Application Note

80000NT10027a Rev. 0 – 2009-05-29

Making machines talk.

APPLICABILITY TABLE

PRODUCT
UC864-E
UC864-G
UC864-WD
UC864-WDU

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Such changes will, nevertheless be incorporated into new editions of this document.

Contents

1 Introduction

1.1 Scope

The aim of this document is the description of some hardware specification useful to develop a product using Telit modules supporting DVI, as specified in the aforementioned applicability table.

1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UC864 modules.

1.3 Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4 Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "UC864 DVI (PCM)" describes the DVI port as far as the UC864 module is concerned

Chapter 4: "Protocol description"

Chapter 5: "Parameters and timing characteristics"

Chapter 6: "Custom AT commands"

Chapter 7: "External codec" provides an example of interfacing with an external audio codec.

1.5 Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6 Related Documents

- UC864 Software User guide, 1vv0300767
- UC864 Hardware User Guide, 1vv0300766a
- UC864 Product description, 80281ST10034a
- UC864-E/G AT Commands Reference Guide, 80304ST1004a

1.7 Document History

Revision	Date	Changes
ISSUE#0	2009-05-29	First release

2 Overview

The Telit Modules support the ***Digital Voice Interface*** (from here onwards ***DVI***), which can be used to transfer digital audio data *to* and *from* the module itself.

The ***DVI*** uses the *PCM interface* as part of the audio front end; it easily allows for an external codec to be used instead of the internal codec.

As an example, through the ***DVI*** you could connect a Telit Module to a Bluetooth device.

2.1 General information

The Telit Modules can have one or two ***DVI*** ports, but only one can be active at the same time.

The choice between them depends from configuration of the alternate functions of the pins of the digital interface in your application.

Please refer to the User Guide of the module that you are using to know the number of the available ***DVI*** ports.

The ***DVI*** ports can be configured as *PCM Interface Master*, generating an output clock of 128 KHz, or *PCM Interface Slave*, operating with input clock of 2.048MHz; they work in burst mode at 8 KHz mono voice data.

The gains (volumes) for DOWNLIK and UPLINK paths can be set:

1. by the dedicated AT commands
2. by tuning the gain of the external codec amplifiers (refer to external codec manual)

The Acoustic Echo canceller is active also when ***DVI*** is activated.

2.2 Hint on PCM

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.

It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.

PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8KHz that means 125 µSec between samples) is required.

3 UC864 DVI (PCM)

The UC864 has only one ***DVI*** port (or *Auxiliary Codec Port*), a hardware support for continual transmission and reception of PCM Data. It has two different modes:

- Standard Operating Mode, actually used
- Standalone Operating Mode, actually not allowed

The activation of the ***DVI function*** does the internal codec automatically disabled, and the user has to interface an external codec (the "*AUXILIARY PCM device*") in order to use it.

Even if the ***Auxiliary Codec Port*** is physically one, you can set it via software in two configuration modes, each one with its own clock frequency, clock format, frame synchronism and clock mode.

3.1 Configuration mode

The configuration modes are ***Auxiliary*** and ***Primary.*** The choice depends from the needs of the customer, but always keeping in mind that only *one mode at time* is allowed.

- ***Auxiliary*** *Configuration Mode* is the *default mode* running at 128 KHz with standard *Long Frame Sync* timing. It supports: *16-bit linear* or *8-bit A-Law* or *µ-Law with padding*.

- ***Primary*** *Configuration Mode* is the *other mode* running at 2.048 MHz with *Short Frame Sync* timing. It supports only: *8-bit A-Law* or *µ-Law with padding*.

A-Law is the PCM variant in Europe, while *µ-Law* is the PCM variant in America.

3.2 Clock Mode

The *clock Mode* is defined:

- ***Master*** if UC864 is the clock signal source; the ***PCM_CLK*** pin becomes an output and its direction is from UC864 to external codec.

- ***Slave*** if the external "*AUXILIARY PCM device*" is the signal clock source; the ***PCM_CLK*** pin becomes an input and its direction is from external codec to UC864

WARNING:

Slave mode is not allowed in the "*AUXILIARY Configuration Mode*".

3.2.1 Interfacing an external stereo DAC

The *AUX_PCM interface* pins can also be used to interface with an external stereo DAC (SDAC) to play stereo sound or music (*MP3 or MIDI for example*).

3.3 Summary

- the *Digital Voice Interface* allows the use of an external codec .It is Software , and can be the "*AUXILIARY PCM Interface*" (*the default interface*) working at 128KHz clock , or the "*PRIMARY PCM Interface*" (*the other interface*) working at 2.048MHz ;
- the "*AUXILIARY CODEC PORT*" operates at 128KHz when the "*AUXILIARY PCM Interface*" is active
- the "*AUXILIARY CODEC PORT*" operates at 2.048MHz when the "*PRIMARY PCM Interface*" is active
- the "*AUXILIARY CONFIGURATION Mode*" sets the clock frequency/sync type to 128KHz/ long sync
- the "*PRIMARY CONFIGURATION Mode*" sets the clock frequency/sync type to 2.048MHz/ short sync
- the "*MASTER Clock Mode*" sets UC864 as clock source
- the "*SLAVE Clock Mode*" sets the external "*AUXILIARY PCM device*" as clock source

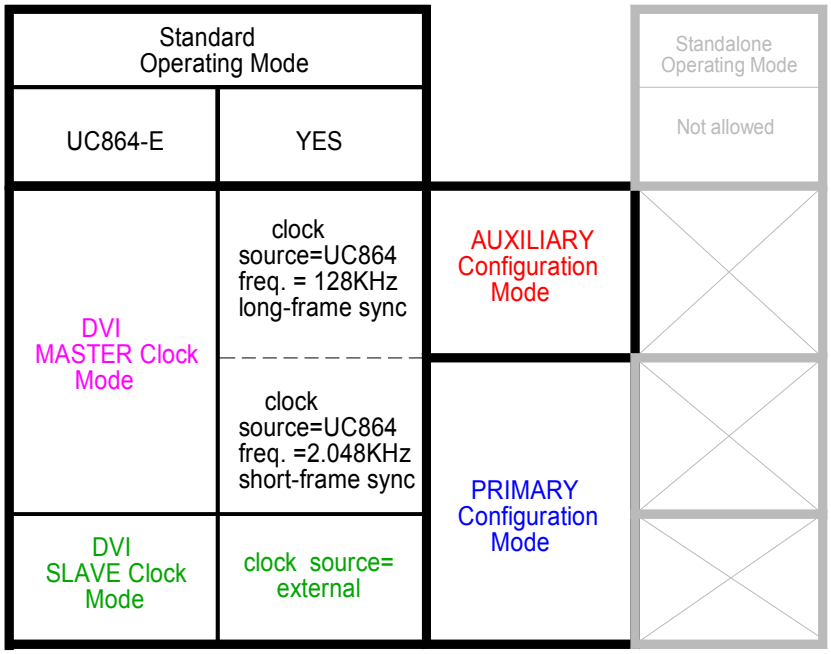

Table 1. Settings Map of the Digital Voice Interface

The DVI interface is accessible on four pins on UC864. The port itself is mapped on two logical ports, Auxiliary port and Primary port, depending on the functionality set via AT command. For the timing diagram of the two different modes, refer to chapter about Protocol Description.

Physical pins			Primary PCM Interface	Auxiliary PCM Interface
number	name	function	name	name
36	AUX_PCM_CLK	clock	PCM_CLK	AUX_PCM_CLK
65	AUX_PCM_DIN	Data in	PCM_DIN	AUX_PCM_DIN
63	AUX_PCM_DOUT	Data out	PCM_DOUT	AUX_PCM_DOUT
71	AUX_PCM_SYNC	synchronism	PCM_SYNC	AUX_PCM_SYNC

Table 2. Signal name Map

3.4 Electrical Characteristics

	Minimum	Maximum	Unit
V_{IL}	**-0.3**	**0.21**	**V**
V_{IH}	**1.69**	2.9	V
V_{OL}	0	0.45	V
V_{OH}	2.15	2.6	V

3.5 Signals routing

The table below summarizes how the *default functions* and *the four useful signals direction* change.

UC 864 PIN	Default Function	DVI Function	Signal	Function		Master Direction	Slave Direction
36	*Dedicated*	PCM_CLOCK	*DVI_CLK*	Data Clock	→	**OUT**	**IN**
71	TGPIO_17	PCM_SYNC	*DVI_SYNC*	Frame Synchronism	→	**OUT**	**IN**
65	TGPIO_18	PCM_RX	*DVI_RX*	Received Data	→	**IN**	**IN**
63	TGPIO_10	PCM_TX	*DVI_TX*	Transmitted Data	→	OUT	OUT

3.6 Pin displacement

Telit offers the dedicated Interface Board ***KS0101***, where the **UC864** could be fitted on during the development phase of the customer application.

The useful ***DVI*** signals are available on two connectors named PL101 and PL102 .

DVI Function	PL101	PL102
PCM_CLOCK		**13**
PCM_SYNC	**19**	
PCM_RX	**17**	
PCM_TX		7

Table3. Pin assignment

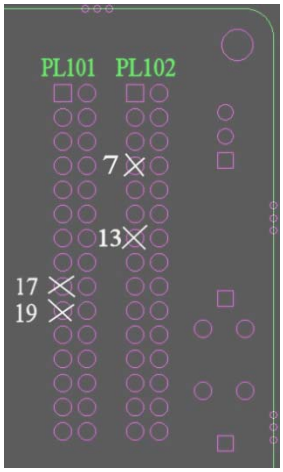

Figure1 . *DVI* Pin displacement on KS0101

4 Protocol Description

The ***DVI*** operates in 16-bit data burst mode, starting with the most significant bit.

GSM voice is 13-bit *2's* complement but the output of the speech decoder is saved on 16-bit *2's* complement (Q15 format). The last 3 LSBs are equal to 0.

The frame lasts for 17 clock pulses, as one more clock pulse is needed for the frame synchronization of the signal ***PCM_SYNC***.

Following the falling edge of the ***PCM_SYNC*** signal, the data bits are sampled at the module data input (RX) and module output data (TX) at the next falling clock (CLK) pulse edge.

All data is 8kHz and 16 bits with DVI (PCM interface).

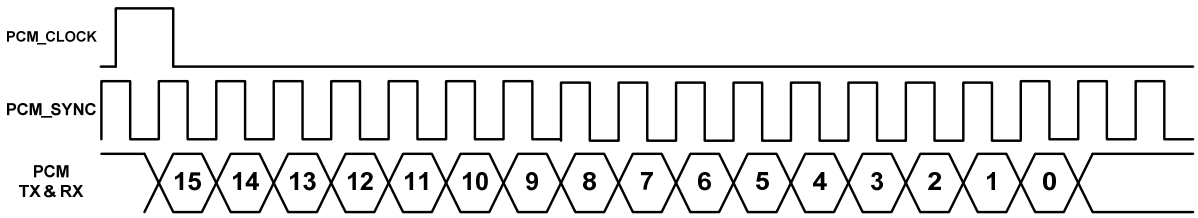

Figure 2. Digital Voice Interface (PCM) signal timing

4.1 Primary Mode

On ***Primary*** mode UC864 provides a 16-bit linear or 8-bit A-law or μ-law with padding, with short-sync and 2.048MHz clock (on the ***PCM_CLOCK*** pin).

Both ***Master*** and ***Slave*** mode are allowed.

4.2 Auxiliary Mode

On ***Auxiliary mode*** UC864 provides only 8-bit A-law or µ-law with padding, with ***long-sync*** and 128KHz clock (on the **PCM_CLOCK** pin).

Only ***Master*** mode is allowed.

5 Parameters and Timing Characteristics

5.1.1 Primary PCM Interface

Parameter	Description	Min	Typical	Max	Units
t(sync)	PCM_SYNC cycle time (SLAVE mode)		125		us
	PCM_SYNC cycle time (MASTER mode)		125		us
t(synca)	PCM_SYNC asserted time (SLAVE mode)	400	500		ns
	PCM_SYNC asserted time (MASTER mode)				ns
t(syncd)	PCM_SYNC de-asserted time (SLAVE mode)		124.5		us
	PCM_SYNC de-asserted time (MASTER mode)				us
t(clk)	PCM_CLOCK cycle time (SLAVE mode)	400	500		ns
	PCM_CLOCK cycle time (MASTER mode)				ns
t(clkh)	PCM_CLOCK high time (SLAVE mode)	200	250		ns
	PCM_CLOCK high time (MASTER mode)				ns
t(clkl)	PCM_CLOCK low time (SLAVE mode)	200	250		ns
	PCM_CLOCK low time (MASTER mode)				
t(susync)	PCM_SYNC setup time to PCM_CLOCK falling (SLAVE mode)		150		ns
	PCM_SYNC setup time to PCM_CLOCK falling (MASTER mode)				ns
t(hsync)	PCM_SYNC hold time after PCM_CLOCK falling (SLAVE mode)		300		ns
	PCM_SYNC hold time after PCM_CLOCK falling (MASTER mode)				ns
t(sudin)	PCM_RX setup time to PCM_CLOCK falling	50			ns
t(hdin)	PCM_RX hold time after PCM_CLOCK falling	10			ns
t(pdout)	Delay from PCM_CLOCK rising to PCM_TX valid			350	ns
t(zdout)	Delay from PCM_CLOCK falling to PCM_TX HIGH-Z		160		ns

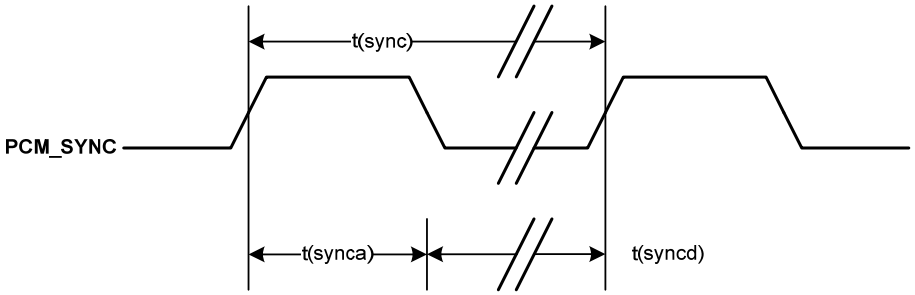

Figure 3. Primary PCM_SYNC timing (only Short sync)

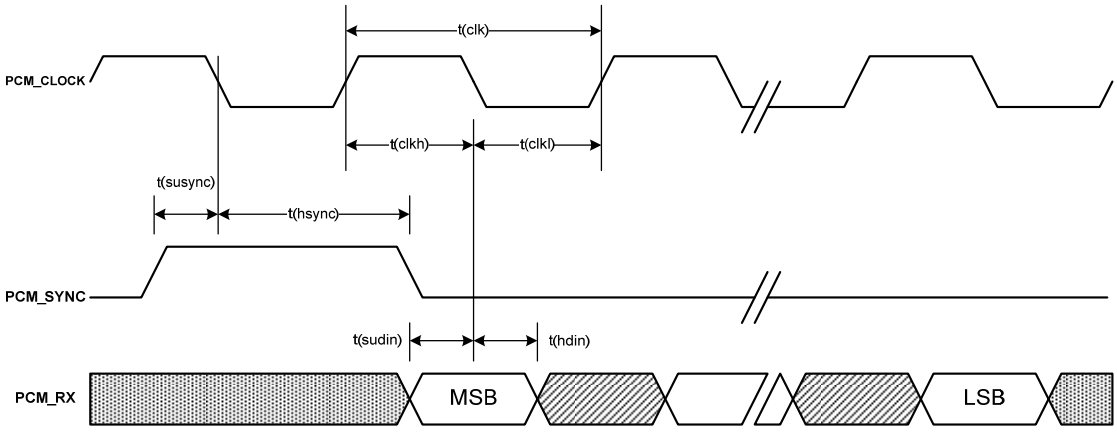

Figure 4. External codec to UC864 timing

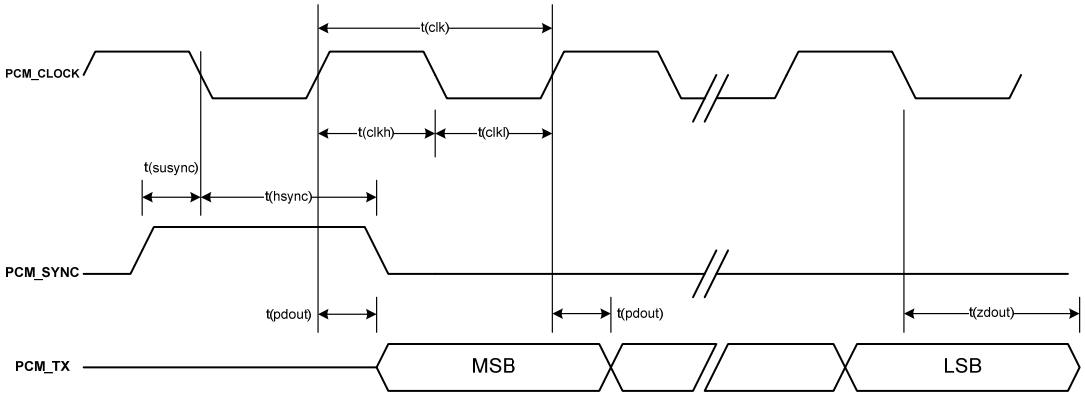

Figure 5. UC864 to External codec timing

5.1.2 Auxiliary PCM Interface

Parameter	Description	Min	Typical	Max	Units
t(auxsync)	PCM_SYNC cycle time		125		us
t(auxsynca)	PCM_SYNC asserted time	62.4	62.5		us
t(auxsyncd)	PCM_SYNC de-asserted time	62.4	62.5		us
t(auxclk)	PCM_CLOCK cycle time		7.8		us
t(auxclkh)	PCM_CLOCK high time	3.8	3.9		us
t(auxclkl)	PCM_CLOCK low time	3.8	3.9		us
t(suauxsync)	PCM_SYNC setup time to PCM_CLOCK rising	1.95			us
t(hauxsync)	PCM_SYNC hold time after PCM_CLOCK rising	1.95			us
t(suauxdin)	PCM_RX setup time to PCM_CLOCK falling	70			ns
t(hauxdin)	PCM_RX hold time after PCM_CLOCK falling	20			ns
t(pauxdout)	Propagation delay from PCM_CLOCK to PCM_TX valid			50	ns

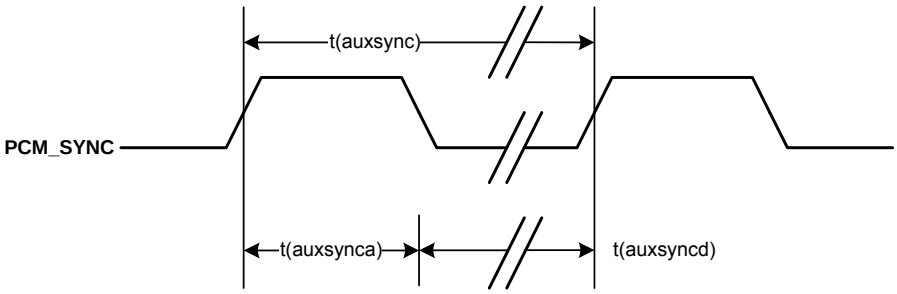

Figure 6. AUX PCM_SYNC timing (only Long sync)

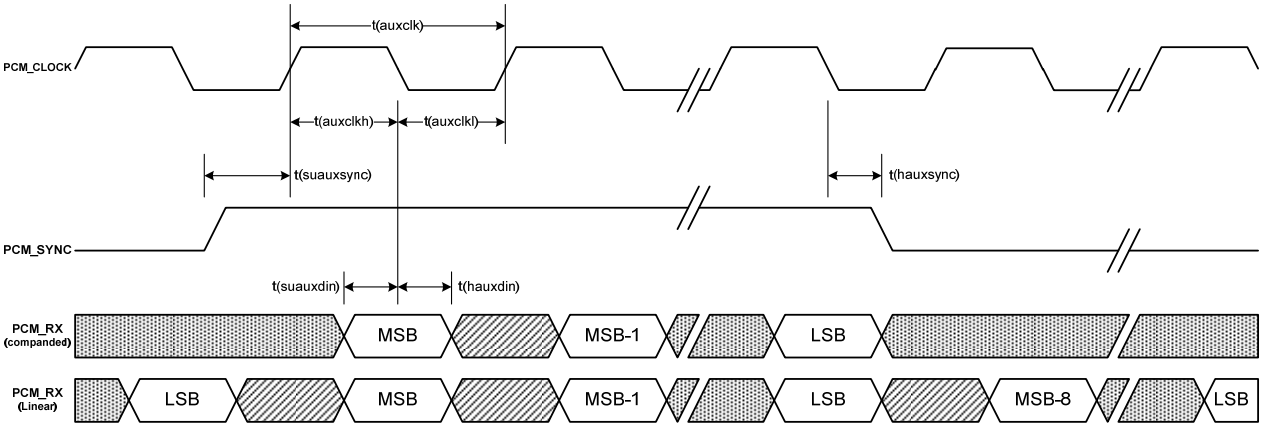

Figure 7. AUX External codec to UC864 timing

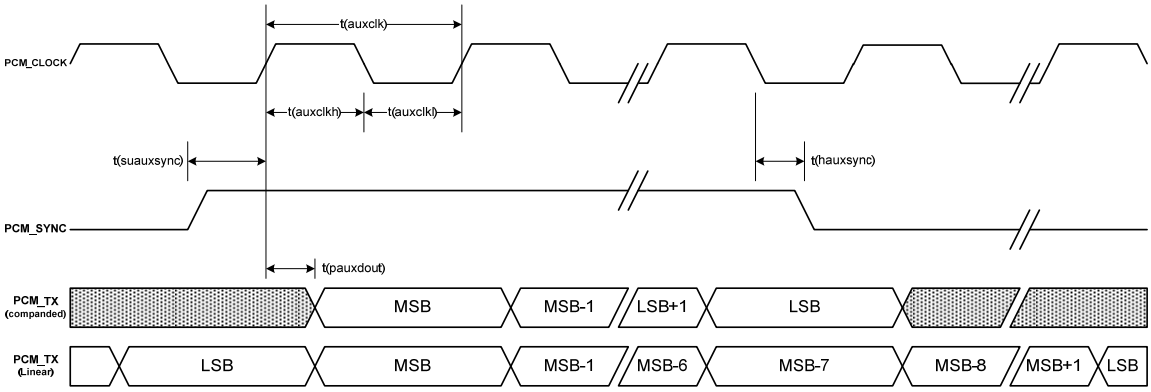

Figure 8. AUX UC864 to External codec timing

6 Custom AT Commands

The ***DVI can*** be set by the following custom ***AT commands*** .
Needing more details, please refer t ***AT_Commands_Reference_Guide_UC864*** Telit specification document.

6.1 DVI port Enabling

AT#DVI	
AT#DVI=<mode> [,<dviport>,<clockmode>]	*Set command*: it enables/disables the Digital Voiceband Interface. Parameters. **<mode>** - activation of DVI. 0 - DVI disabled , factory default Audio is forwarded to the analog line ; DVI pins can be used for any allowed purposes (GPIO, etc) . 1 - enable DVI; audio is forwarded to the DVI block **<dviport>** 2 - DVI port 2 will be used **<clockmode>** 0 - DVI slave 1 - DVI master , factory default Note: **#DVI** parameters are saved in the extended profile
AT#DVI?	*Read command*; it reports the last setting in the format: **#DVI: <mode>,<dviport>,<clockmode>**
AT#DVI=?	*Test command* ; it reports the range of supported values for parameters in the format: **<mode>,<dviport>** and **<clockmode>**
Example	***AT#DVI=1,2,1*** ***OK*** DVI activated for audio. DVI is configured as Master providing on DVI port #2

6.2 DVI port Configuration

AT#DVICFG	
AT#DVICFG= <clock>, <decoder pad>, <decoder format>, <encoder pad>, <encoder format>	*Set command* : it sets the DVI configuration Parameters **<clock> .** Master mode Clock speed 0 : normal mode 1 : high speed mode **<decoder pad>** .PCM padding enable in decoder path 0 : disable 1 : enable **<decoder format>** .PCM format in decoder path 0 : µ-Law 1 : A-Law 2 : linear **<encoder pad>** .PCM padding enable in encoder path 0 : disable 1 : enable **<encoder format>** .PCM format in encoder path 0 : µ-Law 1 : A-Law 2 : linear Note: **#DVICFG** parameters are saved in the extended profile
AT#DVICFG=?	*Test command* ; it returns the supported range of values for para meters in the format: **<clock>, <decoder pad> , <decoder format> , <encoder pad> , <encoder format>**

6.3 DVI gain

DVI Microphone Gain	
AT#PCMTXG= <TX_VOL>	Set command ; it sets the DVI UPLINK Gain Parameter **<TX_VOL>** . PCM TX volume in TX path < TX VOL RANGE> : (-5000) ÷(+1200)
Meaning	TX_VOL is 1/100 dB step, except *-5000* that is mute.
Example	***AT#PCMTXG= -2000*** *means DVI TX VOL=-20dB*
AT#PCMTXG?	*Read command* returns; it reports the current PCM Audio TX value in the format : **#PCMTXG: <TX_VOL>**
AT#PCMTXG=?	*Test command* ;it returns the parameter values supported range in the format: **<TX_VOL>**

DVI Speaker Volume	
AT#PCMRXG= <RX_ VOL>	Set command ; it sets the DVI DOWNLINK Gain Parameter **<RX_VOL>** PCM RX volume in RX path <RX_VOL RANGE> : (-5000) ÷ (+1200)
Meaning	RX_VOL is 1/100 dB step , except *-5000* that is mute
Example	: **AT#PCMRXG= -1200** means *DVI RX VOL=+12dB*
AT#PCMRXG?	*Read command* returns; it reports the current PCM Audio RX value in the forma t: **#PCMRXG: <RX VOL>**
AT#PCMRXG=?	*Test command* ;it returns the parameter values supported range in the format: **<RX VOL>**

7 External Codec

The market offers great variety of audio codecs and, obviously, the customers will choose by itself the device that better fits their application.
Just as an example, in the following we go describing a possible interfacing with an external audio codec.

7.1 The choice

MAXIM ® offers in the same package the ***MAX9851/9853***, two stereo audio CODECs designed to provide a complete audio solution, differing only in the stereo output amplifiers:

- ***MAX9853*** has Stereo Differential Line Output Amplifiers
- ***MAX9851*** has Stereo 1.25W/ 8Ω Class-D Amplifiers

We describe the implementation of ***MAX9853***.

7.1.1 Hint on Class-D amplifier

As said before, the stereo output amplifiers of ***MAX9851*** are *Class-D* stages.

This type of amplifier uses switching technique to achieve a power efficiency more than 90% .
Not only, by this configuration do we not need large transformers and heavy heatsinks, because they are smaller and lighter in weight than an equivalent Class AB amplifier.

The ***Class-D audio Amplifiers*** operate in on/off mode: their output stages reproduce signals with a bandwidth well below the switching frequency, and the losses are minimized allowing each output device to be either fully on or off.

The input signal is converted to a sequence of pulses whose averaged value is directly proportional to the instantaneous amplitude of the signal. The frequency of the pulses is typically ten times or more the highest significant frequency in the input signal. The output of such an amplifier contains unwanted spectral components (*the pulse frequency and its harmonics*) which must be removed by an external passive filter. The resulting filtered signal is then an amplified replica of the input.

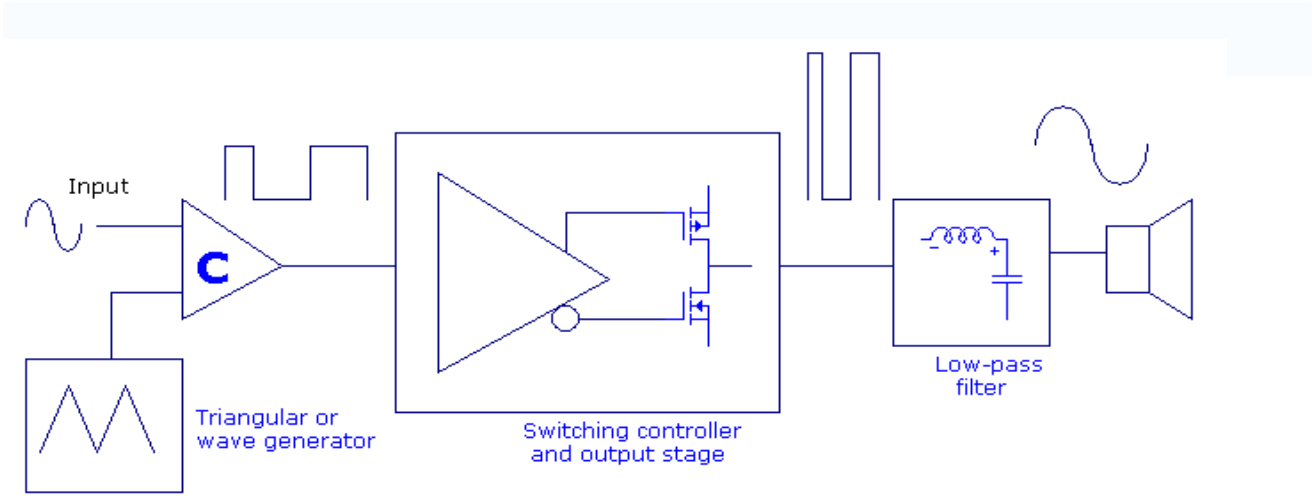

Figure 9 . Block diagram of the Class-D audio Amplifier

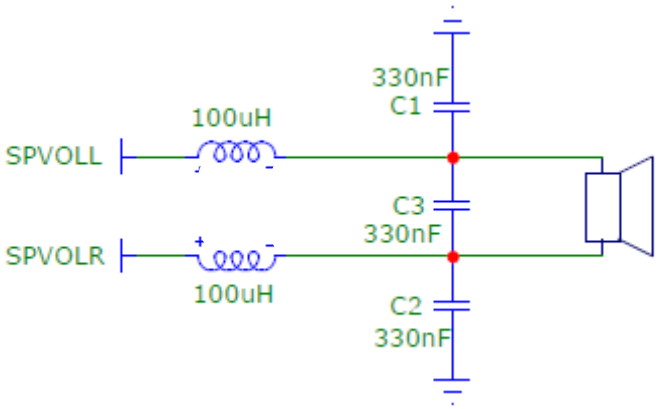

Figure 10. Class-D Low-Pass output filter

7.2 MAX9853 features

MAX9853 audio codec provides:

- stereo amplifiers to directly drive an headset
- a mono (receiver) speaker amplifier
- microphone input amplifiers
- flexible input selection and gain control

Control for volume levels, signal mixing, and operating modes could be applied.

Two "*serial digital audio interfaces"* are at your disposal, one intended to accept *Voiceband Data* and the other to accept *I^2S Data* , supporting a variety of serial audio formats.
The *Voiceband interface* can be reconfigured as needed to act as a secondary *I^2S* feed input, allowing multiple audio sources mixing at different sample rates (*ringer tones and/or other audio inputs*).

The "*secondary serial audio interface"* has independent supply voltages allowing integration into multiple supply systems.

The stereo digital-to-analog converter *(DAC)* path includes:

- filtering and mixing
- programmable-gain amplifiers *(PGA)* on the front end, allowing dynamic range optimization with a wide range of input sources
- soft muting
- optional Voiceband digital filtering

The stereo analog-to-digital converter *(ADC)* converts audio signals from either internal or external microphones or stereo line inputs.
The input amplifiers have a programmable gain ***G=(0 ÷ +40)dB*** , handling both amplified microphones and electret modules.
In addition to a digital highpass filter to remove DC offset voltages, the ADC also features Voiceband digital filtering.

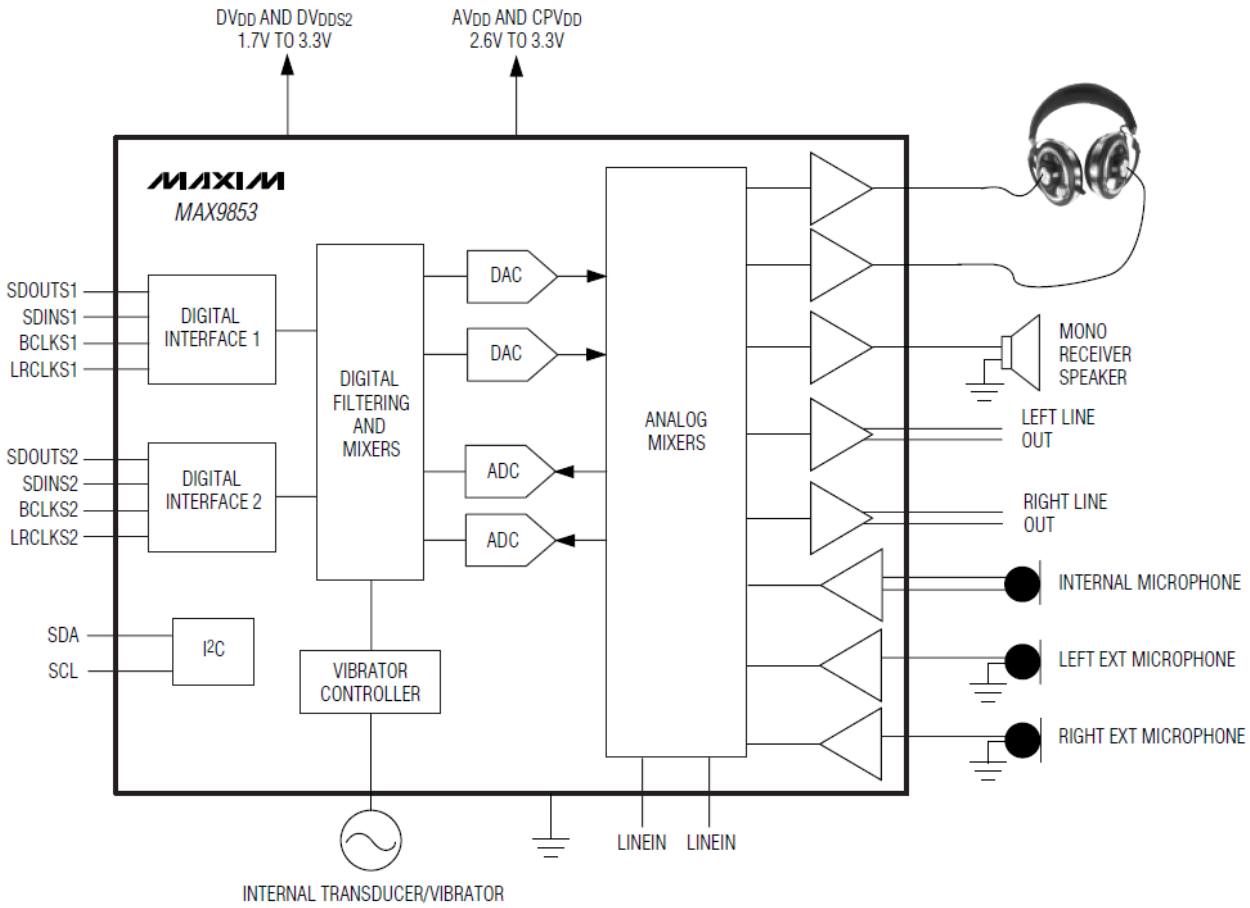

Figure 11. Block diagram of *MAX9853* audio codec

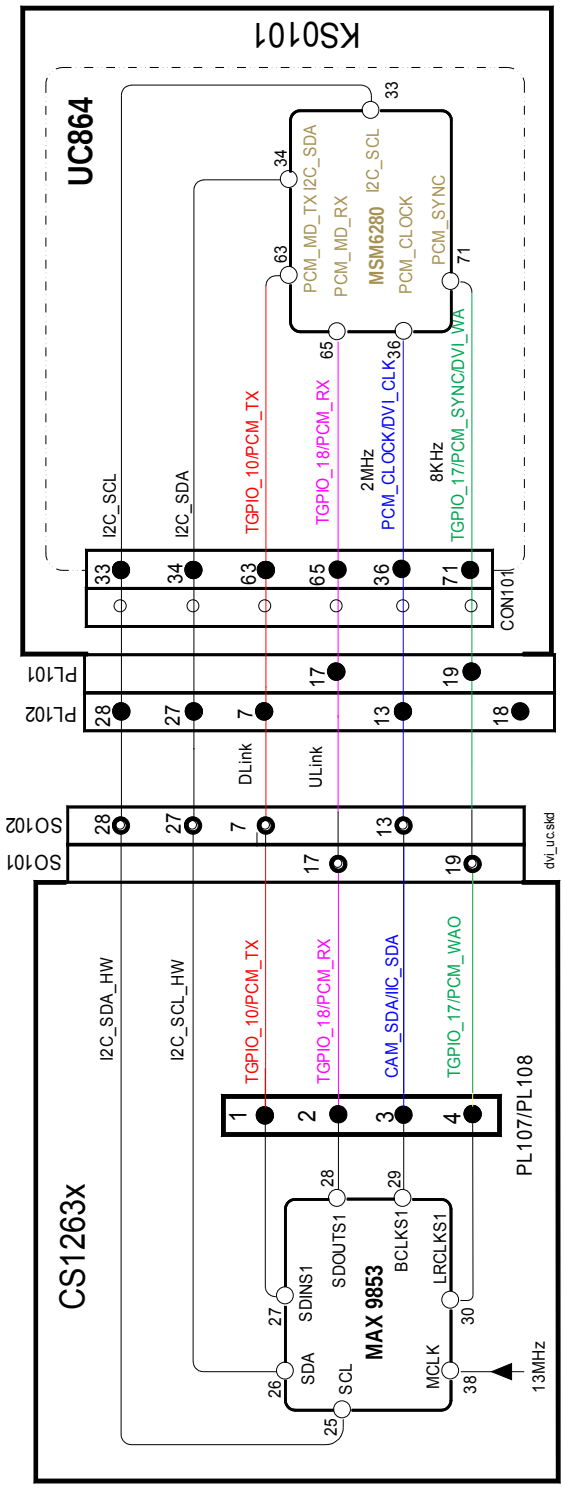

Figure 12. Block diagram of DVI signal routing to/from MAX9853

7.3 Codec and DVI settings

Speaker and microphone are connected to the external output input lines of the codec.
MAX9853 is configured by a script file, sent by a modem like Procomm® or Hyperlink®.
Every block defines some parameters to load:

- amplifiers gain
- signal mixing
- operating mode
- any other information needed

7.3.1 First step DVI signals routing

The DVI useful signals are routed to the assigned pin of the module.
Refer to the Telit module's HW User Guide for all information on the used GPIOs.

- GPIO 10 is PCM_TX
  strfmt command1 "AT#GPIO=10,0,2^M"

- GPIO 17 is PCM_WAO
  strfmt command1 "AT#GPIO=17,0,2^M"

- GPIO 18 is PCM_RX
  strfmt command1 "AT#GPIO=18,0,2^M"

7.3.2 Second step DVI configuration

- Clock rate =2.048 MHz
- PCM decoder padding on
- decoder linear
- PCM encoder padding on
- Encoder linear

strfmt command1 "AT#DVICFG=1,1,2,1,2^M"

7.3.3 Third step MAX9853 configuration

Register address	Data	Description
1a	**d5**	**charge pump on to ext osc**
1b	**02**	**DAC_ADC disabled**
04	**20**	**INTRF1 Codec slave mode,clock polarity**
05	**00**	S2SDI serial INTRF1 off
07	**70**	digital filter default
08	**20**	digital mixer LEFT RIGHT on
0a	**22**	Left ADC IN Mixer Active
0b	**10**	Sidetone off INTRF1 active
0c	**00**	dig audio INTRF1 max gain=0dB
0e	**1f**	min LINE1 in gain -32dB
0f	**1f**	min LINE2 in gain -32dB
10	**20**	Mic L gain +20dB +20dB
12	**06**	on bias L MIC EXT
13	**1f**	SIDETONE gain -32dB
14	**00**	L Amplifier= +6dB
15	**3f**	R Amplifier Mute
16	**7f**	L-Speaker LineOut mute
17	**3f**	R-Speaker LineOut mute
18	**07**	RECEIVER Speaker mode On
0x1a	**0xf5**	shut down off
0x1b	**0xa2**	Left DAC_ADC enabled
0x03	**0xca**	S1SDI serial INTRF1 on mono voice 8KHz

7.3.4 Last step DVI Activation and clock mode setting

- enable DVI; audio is forwarded to the DVI block
- DVI port 2 will be used
- clock mode DVI master

strfmt command1 "AT#DVI=1,2,1^M"

.

7.4 Results

Under the following constraints :

mic input = 5mV$_{rms}$
BSS input = 680mV$_{rms}$
AT#PCMRXG=0
AT#PCMTXG=0

the performance of the UC864, connected to MAX9853 through the ***DVI*** are the same that in ***Analog Voice mode***, that is :

Ear Output=170mV$_{rms}$
MonSpeech Output=3580mV$_{rms}$